**Design of Anti-collision Technique for RFID UHF Tag using Verilog**

**ABSTRACT**

This paper presents a proposed Reliable and Higher Throughput Anti-collision technique (RHTACT) for Radio Frequency Identification (RFID) Class 0 UHF tag. The RHTACT architecture consists of two main subsystems; Pre RHTACT and Post RHTACT. The Pre RHTACT subsystem is to detect any error in the incoming messages. Then the identification bit (ID) of the no error packet will be fed to the next subsystem. The Post RHTACT subsystem is to identify the tag by using the proposed Lookup Table. The proposed system is designed using Verilog HDL. The system is simulated using Modelsim and synthesized using Xilinix Synthesis Technology. The system has been successfully implemented in hardware using Field Programmable Grid Array (FPGA) Virtex II. The output waveforms from the FPGA have been tested on the Tektronix Logic Analyzer for real time verification. Finally the RHTACT architecture is resynthesized using Application Specific Integrated Circuit (ASIC) technology for on-chip implementation. This technology consists of 0.18 μm Library, Synopsys Compiler and tools. From the hardware verification results, it shows that the proposed RHTACT system enables to identify the tags without error at the maximum operating frequency of 80 MHz. The system consumes 13.13mW powers, occupies 11,531 gates and 0.06870 mm area 2 with Data arrival time of 2.72 ns.

**LANGUAGE USED:**

* VHDL/Verilog HDL

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis